



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,914	10/12/2000	Daisuke Sato	107258	5369

25944 7590 02/28/2006

OLIFF & BERRIDGE, PLC  
P.O. BOX 19928  
ALEXANDRIA, VA 22320

EXAMINER

NGUYEN, HAI V

ART UNIT PAPER NUMBER

2142

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b>	Application No. 09/686,914	Applicant(s) SATO ET AL.	
	Examiner Hai V. Nguyen	Art Unit 2142	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 13 February 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 03 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

#### AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 1-4 and 6-12.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

#### AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

#### REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

THONG UU  
P. E.

*[Signature]*

Continuation of 11. does NOT place the application in condition for allowance because: In the remark received on 13 February, Applicant argued in substance that:

Point (1), the prior art does not disclose that, "a data transfer control device for transferring data among a plurality of nodes are connected to a bus, the data transfer control device comprising:

a control circuit which starts transfer processing when processing unit issues a start command for data transfer, and resumes transfer processing when the processing unit issues a resume command for data transfer;  
a transfer execution circuit which executes processing for dividing transfer data into a series of packets then transferring the divided series of packets continuously, when the processing unit issues the start command for data transfer;  
a cancellation circuit which cancels an execution of one of start command and the resume command, when the processing unit issues one of the start command and the resume command, respectively, during a period of a reset that clears node topology information; and  
a circuit which informs the processing unit that command execution has been canceled by the reset.

As to point (1), Wood discloses that, "a data transfer control device (Fig. 1, remote control 22) for transferring data among a plurality of nodes are connected to a bus, the data transfer control device comprising:

a control circuit (Fig. 2, a circuitry 100, components of MPEG decoder subsystem) which starts transfer processing (data recording) when processing unit issues a start command for data transfer (Wood, the components of the MPEG encoder subsystem respond to external commands to stop and start recording, change the recording bit rate, change the encoding resolution, save the current stream position as a bookmark, paragraph [0074]), and resumes transfer processing when the processing unit issues a resume command for data transfer (Wood, the decoder streamer 342 then starts seeking backwards in the video stream until it identifies the beginning of the previous I frame. When the previous I frame is found, the decoder streamer 342 streams forward again, as in play mode, to show at least one complete I frame to the viewer, until it finds the next non-I frame, at which point it starts searching backwards again, past the last found I frame, to the next prior I frame, paragraphs [0032], [0059], [0070]-[0079]).

a transfer execution circuit which executes processing for dividing transfer data into a series of packets then transferring the divided series of packets continuously, when the processing unit issues the start command for data transfer (the OMFS is configured to divide the received digital video information into one or more packets, each packet having the same number of bytes as a sector on a disk in the disk drive, page 1, paragraph [0005]; the digital VCR 10 continuously spools the current show's video and audio streams to a rewind buffer stored on the hard disk drive 142, page 12, paragraphs [0098], [0118]).

a cancellation circuit (the digital VCR 10) which cancels an execution of one of start command and the resume command, when the processing unit issues one of the start command and the resume command, respectively, during a period of a reset that clears node topology information (the personal channel) (Wood, Fig. 4, the digital VCR 10 can determine (by comparing channel guide information for a show that is scheduled to be recorded onto a personal channel with channel guide information for shows that are already recorded on a personal channel) that a show that is scheduled to be recorded onto a personal channel is already stored on the personal channel and/or has already been viewed by the user. In such a case the digital VCR 10 can cancel recording of the show, paragraphs [0022]-[0032], [0097], [0111]) and

a circuit (interrupt handlers 336, 338) which informs the processing unit that command execution has been canceled by the reset (Wood, The two device drivers are responsible for initializing the hardware, enabling direct memory access (DMA) transfers from the hardware into RAM buffers, handling errors, and handling interrupts, paragraph [0074], The MPEG encoder driver 336 (1) performs hardware initialization, such as setting up the encoder 114 to handle the input data resolution and timing, and setting encoding parameters such as bit rate, (2) performs interrupt handling, paragraph [0075]; The decoder driver 338 is responsible for initializing the hardware, enabling DMA transfers to the hardware from RAM buffers, handling errors, and handling interrupts. [0077]).

Point (B), Applicant argued that Wood is silent regarding the existence of node topology, a processing unit that issues start and stop command, or a cancellation circuit which cancels such commands.

As to point (B), the node topology is merely the configuration or layout of a network formed by the connections between devices on network (see MS Computer Dictionary, 4<sup>th</sup> edition) which is shown in figure 1 of Wood, and also

Wood discloses that "the digital VCR 10 can begin recording a show at a selected time (e.g., three minutes) before the show is scheduled to be broadcast and stop recording the show at a selected time after the show is scheduled to finish broadcasting" paragraph ([0096]) or "the digital VCR 10 can cancel recording of the show" paragraph ([0097]).

Point (C), Applicant argued that Wood does not disclose the limitation of "a circuit which informs a processing unit that command execution has been canceled by the reset" in claim 1.

As to point (C), Applicant's abstract discloses that, "the fact that the command has been cancelled is informed to the CPU by an interrupt". Therefore, the claimed limitation of "a circuit which informs a processing unit that command execution has been canceled by the reset" in nothing more the interrupt handling which is performed by the MPEG encoder driver 336 and the decoder driver 338 in paragraphs [0074]-[0077] of Wood.